What is claimed is:

1. A multi-layer substrate structure for reducing layout area, comprising:

a first core layer, including a first surface connected to a power supply layer and a second surface corresponding to the first surface;

a second core layer, including a third surface connected to a first grounding layer and a fourth surface corresponding to the third surface; and

a set of coupled transmission lines, including a plurality of first differential signal lines formed on said second surface with a certain line width and a plurality of second differential signal lines formed on said fourth surface with the line width corresponding to said first differential signal lines;

wherein, said second surface and said fourth surface are connected to a first dielectric layer making said second surface separated from said fourth surface with a first distance, and said first differential signal lines as well as said second differential signal lines are oppositely overlapped with at least a portion of said signal line width.

2. The multi-layer substrate structure for reducing layout area recited in claim 1, wherein said first dielectric layer packs said set of coupled transmission lines, making said first differential signal lines separated from said second differential signal lines with a second distance.

3. The multi-layer substrate structure for reducing layout area recited in claim 1, wherein said multi-level stack structure further comprises:

a third core layer, including a fifth surface connected to a second grounding layer and a sixth surface corresponding to said fifth surface;

a signal transmission line layer, connected to said sixth surface; and

a second dielectric layer, connected to said sixth surface and said power supply layer.

4. The multi-layer substrate structure for reducing layout area recited in

claim 3, wherein said signal transmission line layer further includes a plurality of signal transmission lines with appropriate arrangement.

5. The multi-layer substrate structure for reducing layout area recited in claim 3, wherein said second dielectric layer packs said signal transmission line layer, making said power supply layer separated from said signal transmission line layer with an third distance.

6. The multi-layer substrate structure for reducing layout area recited in claim 3, wherein on said first grounding layer and said second grounding layer are respectively covered with a covering structure, including:

a second dielectric layer, connected to said grounding layer;

a signal layer, connected to said second dielectric layer; and

a Solder mask layer, covering and connecting to said signal layer.

7. A multi-layer substrate structure for reducing layout area, comprising:

a first stack structure, including:

a first core layer, including a first surface connected to a power supply layer and a second surface corresponding to said first surface;

a second core layer, including a third surface connected to a first grounding layer and a fourth surface corresponding to said third surface;

a first set of coupled transmission lines, including a plurality of first differential signal lines formed on said second surface with a certain line width and a plurality of second differential signal lines formed on said fourth surface with the line width corresponding to said first differential signal lines; and

a first dielectric layer, connected to said second surface and said fourth surface to make said first differential signal lines and said second differential signal lines overlapped oppositely with at least a portion of said signal line width, and further packing said first set of coupled transmission lines to make said first differential signal lines and said second differential signal lines apart from a first distance; and

a second stack structure, including:

a third core layer, including a fifth surface connected to said power supply layer and a sixth surface corresponding to said first surface;

a fourth core layer, including a seventh surface connected to a second grounding layer and a eighth surface corresponding to said seventh surface;

a second set of coupled transmission lines, including a plurality of third differential signal lines formed on said sixth surface with a certain line width and a plurality of fourth differential signal lines formed on said eighth surface with the line width corresponding to said third differential signal lines; and

a second dielectric layer, connected to said sixth surface and said eighth surface to make said third differential signal lines and said fourth differential signal lines overlapped oppositely with at least a portion of said signal line width, and further packing said second set of coupled transmission lines to make said third differential signal lines and said fourth differential signal lines apart from a second distance.

8. The multi-layer substrate structure for reducing layout area recited in claim 7, wherein on said first grounding layer and said second grounding layer are respectively covered with a covering structure, including:

a second dielectric layer, connected to said grounding layers;

a signal layer, connected to said second dielectric layer; and

a Solder mask layer, covering and connecting to said signal layer.

9. The multi-layer substrate structure for reducing layout area recited in claim 7, wherein said first stack structure is connected to another second stack structure to make said first grounding layer of said first stack structure combined with the second grounding layer of said another second stack structure, and said another second stack structure is connected to another first stack structure with another power supply layer.

10. The multi-layer substrate structure for reducing layout area recited in claim 9, wherein on said second grounding layer of said second stack structure and the first grounding layer of said another first stack structure are respectively covered with a covering structure, including:

a second dielectric layer, connected to said grounding layer;

a signal layer, connected to said second dielectric layer; and

a Solder mask layer, covering and connecting to said signal layer.

11. The multi-layer substrate structure for reducing layout area recited in claim 7, wherein said second stack structure is connected to another first stack structure to make said second grounding layer of said second stack structure combined with the first grounding layer of said another first stack structure, and said another first stack structure is connected to another second stack structure with another power supply layer.

12. The multi-layer substrate structure for reducing layout area recited in claim 9, wherein on said first grounding layer of said first stack structure and the second grounding layer of said another second stack structure are respectively covered with a covering structure, including:

a second dielectric layer, connected to said grounding layer;

a signal layer, connected to said second dielectric layer; and

a Solder mask layer, covering and connecting to said signal layer.